IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Eric David Blom

Patent No.: 7,088,139

Issued: August 8, 2006

For: LOW POWER TRI-LEVEL DECODER
       CIRCUIT

REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.322

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted several errors which should be corrected.

In the Specification:

First Page Col. 2 (U.S. Patent Documents), Line 2, After "6,472,907" delete "B1" and insert -- B2 --.

First Page Col. 2 (U.S. Patent Documents), Line 3, After "6,700,416" delete "B1" and insert -- B2 --.

First Page Col. 2 (U.S. Patent Documents) Line 4, After "6,864,725" delete "B1" and insert -- B2 --.

Column 2, Line 62, After "current" delete "11" and insert -- I1 --.
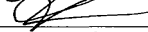
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The errors were not in the application as filed by applicant; accordingly no fee is required. Enclosed please find marked up copies of Notice of References Cited (2) pages and a copy of the Specification.

Transmitted herewith is a proposed Certificate of Correction effecting such amendment. Patentee respectfully solicits the granting of the requested Certificate of Correction.

Dated: October 12, 2006   Respectfully submitted,

By _____
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

Page __1__ of __1__

PATENT NO. : 7,088,139

APPLICATION NO. : 10/750,375

ISSUE DATE : August 8, 2006

INVENTOR(S) : Eric David Blom

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:

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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,201,378 B1	03-2001	Eto et al.	323/313
	B	US-6,864,725 B2	03-2005	Cowles et al.	327/108
	C	US-6,472,907 B2	10-2002	Setogawa, Jun	326/83
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited	Application/Control No.	Applicant(s)/Patent Under Reexamination	
	10/750,375	BLOM, ERIC D.	
	Examiner	Art Unit	Page 1 of 1
	Daniel D. Chang	2819	

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,700,416 B2	03-2004	Cowles, Timothy B.	327/74
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
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	J	US-			
	K	US-			
	L	US-			
	M	US-			

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U.S. Patent and Trademark Office
PTO-892 (Rev. 01-2001)   **Notice of References Cited**   Part of Paper No. 20051111

Current mirror circuit 122 is configured to receive a first switch current (I1) at node N4. Current mirror circuit 122 is further configured to reflect current I1 to provide a first reflected current (I2) at node N5 according to a pre-determined ratio (A). Preferably, the ratio (A) is greater than one-to-one. According to one example, the ratio (A) is three-to-one such that I2 is approximately three times greater than I1.

Switch circuit 104 is configured to also receive voltage VCTL. Switch circuit 104 is further configured to isolate node N7 from node N6 if voltage VCTL exceeds a high threshold. Switch circuit 104 is further configured to reduce a resistance between node N6 and node N7 otherwise.

Current mirror circuit 124 is configured to receive a second switch current (I3) at node N7. Current mirror circuit 124 is further configured to reflect current I3 to provide a second reflected current (I4) at node N8 according to another pre-determined ratio (B). According to one example, B is the same as the pre-determined ratio (A). Alternatively, the ratio (A) may be different from the other ratio (B).

Driver circuit 130 is configured such that if node N2 does not receive an input signal strong enough to drive node N2, driver circuit 130 actively drives node N2 so that node N2 is not floating. Driver circuit 130 is configured to drive node N2 to a voltage between the low threshold and the high threshold if node N2 does not receive a driving input signal. Node N2 will receive a driving input signal from node N1 if node N1 is driven to an active high logic level or an active low logic level. Node N2 will not receive a driving input signal if node N1 is left floating.

Circuit 100 receives an input signal (IN) at node N1. Signal IN has an associated voltage (VIN). According to one implementation, circuit 100 is configured to detect whether node N1 has been actively pulled high, actively pulled low, or left floating, and to produce a corresponding two-bit digital output, with one bit each at nodes N5 and N8. According to an alternative implementation, circuit 100 is configured to detection with node N1 is actively pulled high, actively pulled low, or driven to an intermediate voltage level. Circuit 100 is arranged to provide signal OUT0 at node N5 and signal OUT1 at node N8. Signal OUT0 has a corresponding voltage (VOUT0), and signal OUT1 has another corresponding voltage (VOUT1). Signal OUT0 corresponds to a logic low if node N1 actively driven low. Signal OUT0 corresponds to a logic high if node N1 is

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